

OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH  
PERFORMANCE BALL GRID ARRAY PACKAGES

**CROSS REFERENCE TO RELATED APPLICATIONS**

This application is related to provisional application Serial No. 60/046,062 (TI-22215), the contents of which are incorporated herein by reference and is a division of Serial No. 09/250,641, filed February 16, 1999 and priority claimed therein.

**BACKGROUND OF THE INVENTION**

**FIELD OF THE INVENTION**

This invention relates to a method of laying out traces on a substrate and the layout for connection of a semiconductor chip to a printed wiring board and the like.

**BRIEF DESCRIPTION OF THE PRIOR ART**

Semiconductor integrated circuits are formed in semiconductor chips which contain the electrical circuits. Bond pads are generally disposed on the chip with the chip being mounted within a package and the bond pads being connected by wires to lead frame fingers or the like

which extend externally of the chip. The package, after fabrication, is generally secured to a printed wiring board with the lead frame fingers or the like connected to bonding regions on the printed wiring board. The package as well as the electrically conductive members which transfer the signals from the chip to the printed wiring board add to the undesirable loads (i.e., inductances, noise, crosstalk, etc.) which the chip may see with the magnitude of these undesirable loads increasing with increasing chip operating frequency.

A typical package may include a substrate having a cavity which contains a chip within the depression. Bond wires couple bond pads on the chip to individual copper traces on the substrate, the copper traces each extending to an electrically conductive aperture or via which extends through the substrate to an electrically conductive ball pad and a solder ball. The vias and ball pads are formed in a matrix array having plural rows and columns of vias which are located adjacent one or more of the sides defining the depression. Adjacent vias and ball pad centers in a row or a column are spaced apart from each other by a distance defined herein as a "ball pitch", this distance being the dimension from the center of one via or ball pad to the center of the adjacent via or ball pad in the same row or in the same column. The "ball pitch" between all adjacent vias or ball pads in the same row or in the same column is the same. The solder ball is soldered to a pad on a printed wiring board in standard manner as discussed in the above noted copending application to make the connection from the chip to the printed wiring board pad.

The copper traces as well as the bond wires, electrically conductive regions in the vias and surrounding wiring and packaging add additional circuitry to the electrical circuit which bring to the circuit additional resistances, inductances and capacitances. The layout of the circuitry and



## SUMMARY OF THE INVENTION

In accordance with the present invention, the above described problems of the prior art are minimized.

Briefly, the path traversed by each trace of each differential wiring pair is adjusted to have a pitch or distance therebetween substantially equal to or less than a ball pitch as defined hereinabove, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same cross-sectional geometry to the closest extent possible. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) substantial identity of geometry and spacing between the cross-sections of the two traces forming the differential pair. It is also necessary that each trace of the differential pair be equally spaced from the ground plane, if present, and be tailored to provide maximal performance with respect to the ground plane. The geometry of design is set up to match odd/even mode circuit impedance. Accordingly, the dielectric constant of the substrate separating the signal plane from the ground plane can be controlled to control the impedance in the signal lines as is well known. The geometric relationship between the width, separation, thickness and distance from the ground plane of the conductors also affects the impedance of the conductors.

In the present state of the art, it is possible to provide at most two signal traces between a pair of adjacent columns at minimum ball pitch. In order to meet the above criteria, it has been

found that the above described maximization is obtained, with reference to FIGURE 4, by connecting pairs in the manner 1-2, 1-2 and 3-3. This means that, given three adjacent columns 0, 1, 2 and three rows of vias 1, 2, 3 or connection locations in those columns, a first pair of traces will be connected to rows 1 and 2 of a column 1 with the trace connected to row 2 travelling between the columns 0 and 1, a second pair of traces will be connected to rows 1 and 2 of column 2 with the trace connected to row 2 extending between columns 2 and 3 and a third pair of traces which pass between columns 1 and 2 and are connected to the third row in each of these columns. In the event the technology permits more than two traces to be passed between a pair of adjacent rows, the above manner of connection would be altered, as is apparent.

It should be understood that, though the above described circuit has been laid out to accommodate differential pairs, each trace of each differential pair can be used to accommodate other types of signals.

It should be understood that the above described layout of signal traces can also be provided wherein the ball grid array is disposed on the same surface as the as the signal trace layout with the vias being eliminated, similar to the embodiment of FIGURE 3 and in the above referenced copending application but with the additional column and connections thereto as in the subject specification.

Advantages of the layout in accordance with the present invention are: improved electrical performance, suitability for high frequency applications and flexibility to use nearly all signal traces as differential pairs or single ended lines. Crosstalk is also substantially reduced.

[illegible]

FIGURE 2 is a cross sectional view of a portion of the package of FIGURE 1 connected to a printed wiring board;

FIGURE 4 is a preferred layout using three rows of vias for connection to the chip and a pair of traces between each pair of columns of vias.

## **DESCRIPTION OF THE PREFERRED EMBODIMENT**

Referring to FIGURE 1, there is shown a typical package which can be used in accordance with the prior art as well as in accordance with the present invention. The package is shown with the encapsulation removed and includes a substrate 1 having a depression 3 which contains a chip 5. Bond wires 7 couple bond pads 8 on the chip 5 to individual copper traces 9 on the substrate, the copper traces each extending to an electrically conductive aperture or via 11 which extends through the substrate to a solder ball pad 12 and solder ball 13 as shown in FIGURE 2. The vias 11 and solder pad 12 are formed in a matrix array, there being plural rows and columns of vias which can be located adjacent one or more of the sides defining the depression 3. The solder ball 13 is soldered to a pad 15 on the printed wiring board 17 in standard manner as discussed in the above noted copending application to make the connection from the chip 5 to the printed wiring board terminal. While the traces 9 are shown on only one layer, it should be understood that there can be plural layers of signal traces separated by electrically insulating layers with vias extending from the top or interior layer of the substrate to the lower layer which contains ball pads and may also contain circuitry for additional electrical connections from the chip through substrate circuitry to the solder balls connected to the printed wiring board.. It should be understood that the above described layout of signal traces and substrate circuitry may also be inverted in a "cavity-down" configuration such that the solder balls are connected to the same side of the substrate as the chip.

The copper trace 9 as well as the bond wires 7, electrically conductive region in the via 11 and surrounding wiring add additional circuitry to the electrical circuit which bring to the circuit additional resistances, inductances and capacitances. The layout of the circuitry and especially the

traces 9 materially affect the performance of the chip, this being particularly material in the case of differential wiring pairs wherein pairs of wires carry the same or similar signals but are out of phase with each other. In accordance with the present invention, the path traversed by each trace 9 of each differential wiring pair is adjusted to have a pitch or distance therebetween from trace center line to trace center line of up to one solder ball 13 pitch, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same cross-sectional geometry to the closest extent possible. The pitch of the solder ball is set by the industry for the size of the package being used and varies, depending upon package size. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) identity of cross-sectional geometry and spacing between the two traces forming the differential pair. It is also necessary that each trace of a differential pair be equally spaced from the ground plane.

In the present state of the art, it is possible to provide at most two signal traces between a pair of adjacent rows at minimum ball pitch. In order to meet the above criteria, it has been found that the above described maximization is obtained by connecting pairs in the manner 1-2, 1-2 and 3-3 as shown in FIGURES 3 and 4. In the event more or less than two traces can be or are passed between a pair of adjacent rows, the above manner of connection would be altered as is apparent.



[illegible]

✓